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(56) Documents Cited

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(54) Abstract Title

Circuit board via connections

(57) A "Gatling gun" via to interconnect circuit from a first side of a substrate or printed circuit board, to a second side of the substrate or board. The present via structure comprises a center conductor via 130 surrounded by a plurality of ground vias (eg 132, 134). The plurality of ground vias shield the center conductor via, thus providing electrical isolation for the conductor via from the rest of the circuitry. In one embodiment, the conductor via is electrically connected to a conductive pattern on the substrate by a wire bond.

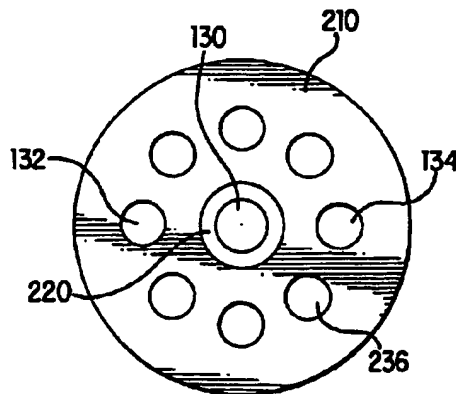


FIG.2

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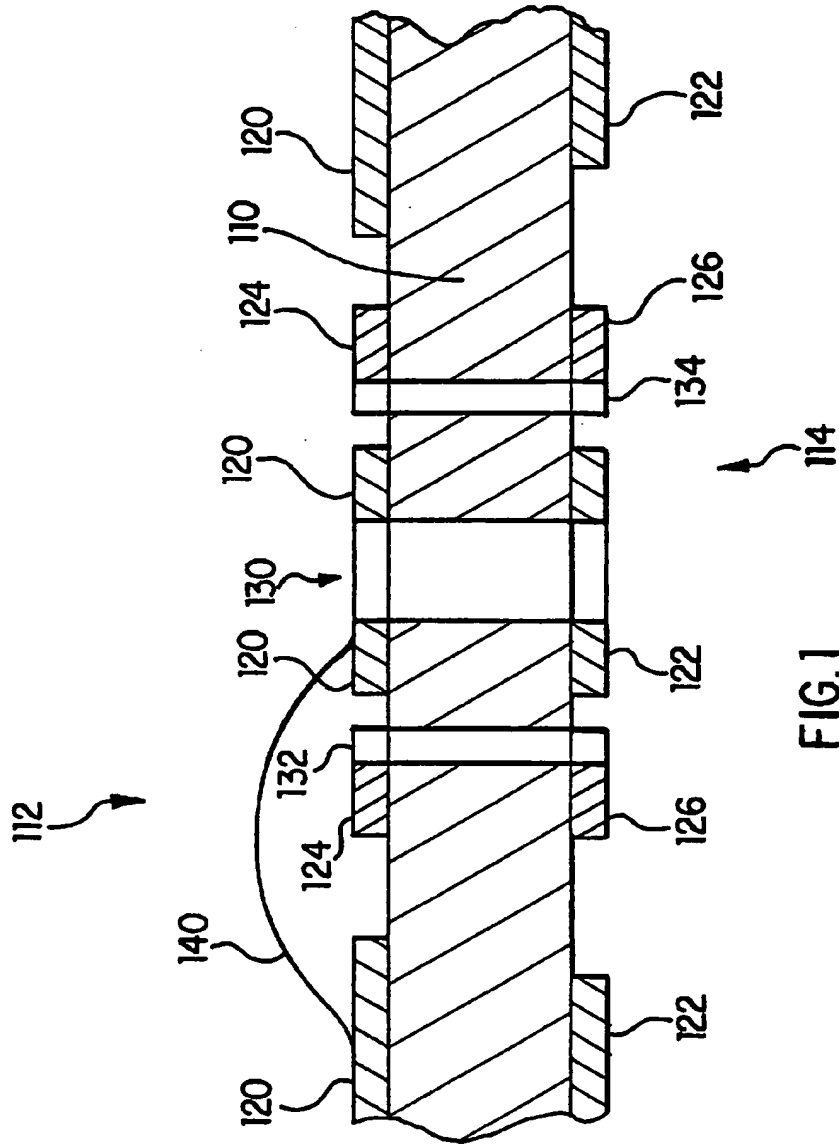


FIG.1

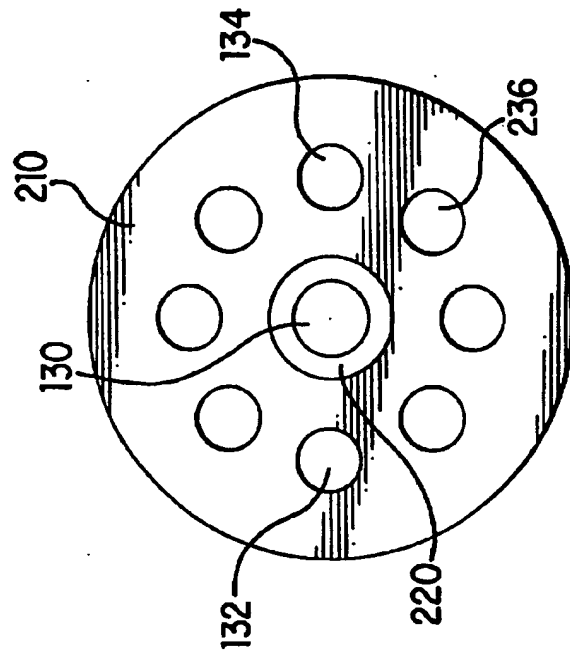


FIG. 2

**A MICROCIRCUIT SHIELDED, CONTROLLED IMPEDANCE
"GATLING GUN" VIA**

FIELD OF THE INVENTION

The present invention relates generally to microcircuits and more particularly to a "Gatling gun" via, that is a via having a center conductor via surrounded by ground vias.

BACKGROUND OF THE INVENTION

Today's complex integrated circuits typically employ of several million transistors on a single integrated circuit substrate. Multiple layers of conductive material are formed overlying the substrate in order for these millions of transistors to interconnect and work as a whole. To facilitate electrical communication between conductive layers, via structures are used. Vias are openings etched through dielectric layers between a first conductive layer and a second conductive layer.

Circuit board interconnects generally fall into three categories. The first category employs a laminated epoxy-filled cloth. The individual layers have electronically conductive paths of patterned copper. The second category uses a base structure of epoxy filled-cloth. This base is then covered with multiple layers of photoimageable dielectric and patterned copper. The third category is composed of multiple layers of laminated ceramic, with individually patterned copper. The present invention is directed to the formation of "Gatling gun" vias with reference to the

second category, although the concepts herein can apply to the other two interconnect schemes.

Vias can be formed by drilling holes and then plating the paths through the holes. The via holes can extend through the complete multilayer board. In this configuration, the vias are electrically coupled to each copper (i.e., conductive) layer. Alternatively, vias can be formed using a conventional photoimage-generated via structure.

One problem with via structures employed in high frequency applications is the lack of AC electrical isolation between the via and the remainder of the microcircuit. Another problem is that standard vias (formed either by drilling or by photoimaging) do not provide a controlled impedance environment at high frequencies.

SUMMARY OF THE INVENTION

The present invention provides a "Gatling gun" via to interconnect circuitry from a first side of a substrate or printed circuit board, to a second side of the substrate or board. The present via comprises a center conductor via surrounded by a plurality of ground vias. The plurality of ground vias shield the center conductor via, thus providing electrical isolation for the conductor via from the rest of the circuitry. One feature of the present invention is that the plurality of ground vias can be modified, adjusting their diameters and their placement relative to the center conductor

via, in order to affect the overall characteristic impedance of the Gatling gun via. This feature is useful when propagating high frequency signals from the first side to the second side of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic cross-sectional view of a laminated epoxy core structure with a Gatling gun via according to the present invention.

FIG. 2 shows a top view of the Gatling gun via.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Richard J. Gatling was born in 1818 in North Carolina, U.S.A. In his early 20s, Gatling invented and improved upon many agricultural implements, including a machine for sowing cotton and a steam-driven plow. But Gatling is probably best remembered for inventing a rapid-firing gun that bears his name.

Following the outbreak of the American Civil War, Gatling became interested in firearms. In 1862 he patented the hand-crank, rapid fire Gatling gun. The first Gatling gun has six rifle barrels mounted around a central shaft. The barrels rotated around the shaft while the gun was operating. Each barrel was mechanically loaded once at the top of a rotation and fired once at the bottom of a rotation. The empty shell was ejected as the barrel advanced up towards a reload. Early models of the Gatling gun fired approximately 300 rounds per minute. By 1882, Gatling improved upon his design so that the gun fired 1200 rounds per minute.

The design of the Gatling gun inspires the present invention. The model of a plurality of barrels around a central shaft is adopted in an improved via structure that provides better isolation and improved controlled impedance for electrically interconnecting circuitry from a first side of a substrate or printed circuit board, to circuitry on a second side of the substrate or board. The discussion below will disclose the present invention in a printed circuit board environment. But one skilled in the art will appreciate the present invention's applicability in a wide variety of applications, including single layer and multi-layer substrates and ceramic.

FIG. 1 shows a schematic cross-sectional view of a laminated epoxy core structure with a Gatling gun via. A base or core laminate of multiple epoxy-filled cloth layers 110 has formed on its topside 112 a pattern of electrically conductive copper 120 while on its backside 114, another pattern of electrically conductive copper 122 is formed. Patterns of copper (items 124 and 126) are also formed on the laminate 110 which are electrically tied to ground as will be discussed more fully below. The patterns (items 120, 122, 124 and 126) are generally disposed in x- and y-direction planes.

The cross section also shows three drilled holes at 130, 132 and 134 extending through the base laminate 110 as well as the copper patterns 120,122, 124 and 126. Holes 130, 132 and 134 are generally disposed in a z-direction, interplanar to the patterns 120,122, 124 and 126.

Once the holes are drilled, a dry film (not shown) can be vacuum laminated to the backside 114 in a conventional manner. The hole at 130 is then filled with conductive, plateable and solderable polymer (not shown) which can be applied as a paste or liquid in a conventional manner. The polymer is then cured and the dry film is stripped. This then forms the center conductor via at 130. In a similar manner, the holes at 132 and 134 are filled and cured.

A wire bond 140 electrically connects the center conductor via 130 to the electrically conductive pattern 120. In another preferred embodiment, the wire bond 140 could be a ribbon bond or dielectric tape or any material that will be able to propagate an electrical signal from the center conductor 130, over the ground via 132 to the electrically conductive pattern 120.

FIG. 2 shows a top view of the Gatling gun via according to the present invention. The center conductor via 130 is surrounded by a plurality of ground vias 132, 134 and 232. A space 220 isolates the conductor via 130 from a ground plane 210 which electrically grounds the plurality of ground vias 132, 134 and 236.

FIG. 2 illustrates the center conductor 130 being surrounded by eight ground vias. This number is not terribly important. Isolation could be accomplished with as little as two vias. Increasing the number of ground vias, increases electrical isolation. Controlling the impedance of the structure is accomplished by varying the diameters of the conductor and ground vias, as well as their relative position from each other. One benefit of the present invention is that propagation of signals in a package

employing the Gatling gun vias is enhanced while minimizing cross talk between signal conductors and power distribution noise. Use of the Gatling gun via also permits the circuit designer to tighten the space between two circuit regions, for example.

What is claimed is:

1. A interconnection structure to connect a first side of a circuit board to a second side of the circuit board, the structure comprising:

a center conductor via 130; and

a plurality of ground vias 132,134, said plurality of ground vias substantially surrounding the conductor via,

wherein the conductor via propagates electrical signals from the first side 112 to the second side 114 of the circuit board.

2. The interconnection structure of claim 1, further comprising:

a wire bond 140, the wire bond electrically connected to the conductor via at a first end and a conductive pattern 120 at a second end.

3. A interconnection structure to connect a first side of a substrate to a second side of the substrate, the structure comprising:

a center conductor 130 via;

a plurality of ground vias 132,134, said plurality of ground vias substantially surrounding the conductor via, and

a wire bond 140, the wire bond electrically connected to the conductor via at a first end and a conductive pattern 120 at a second end, the conductive pattern formed on the first side 112 of the substrate,

wherein the conductor via propagates electrical signals from the first side 112 to the second side 114 of the substrate.



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Claims searched: 1-3

Examiner: SJ Morgan
Date of search: 11 February 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1R (RAN)

Int Cl (Ed.7): H05K 1/20

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	EP 0 318 311 A (GENERAL ELECTRIC) See whole document.	1-3
P, X	US 5 842 877 (ERICSSON) See whole document.	1-3
X	US 4 494 083 (ERICSSON) See whole document.	1-3
X	US 3 895 435 (RAYTHEON) See whole document.	1-3
X	JP 5 206 678 A (NEC) See abstract.	1-3

X Document indicating lack of novelty or inventive step
Y Document indicating lack of inventive step if combined with one or more other documents of same category.

& Member of the same patent family

A Document indicating technological background and/or state of the art.
P Document published on or after the declared priority date but before the filing date of this invention.
E Patent document published on or after, but with priority date earlier than, the filing date of this application.